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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/392,865	09/09/1999	SHOTA KITAMURA	005702-20035	1909

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HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER
TRAN, THIEN F

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/392,865	KITAMURA ET AL.	
	Examiner	Art Unit	
	Thien F Tran	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09-23-2002 has been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 18-21 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The recitation of the second silicon nitride layer not exist on the source/drain diffusion layers sets forth structure not supported by the application. Applicant is requested to point out wherein the application the provides such support. Fig. 2a shows the second silicon nitride layer 11 do exists on said source/drain diffusion layers (7a, 7b).

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 18-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Because of plural recitations of the limitation "layer" in the claims, it is unclear which layer is removed by etching.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 18, insofar as in compliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehrad et al. (USPN 6,071,779) in view of Mori (JP 407161848).

Mehrad et al. discloses a nonvolatile semiconductor memory device (Figs. 2) comprising a semiconductor substrate 52; shallow trench isolation layers 70 which are strip shaped, extending in one direction, and embedded in a surface of said semiconductor substrate with predetermined intervals, a strip-shaped memory region being formed between two adjacent shallow trench isolation layers, and two adjacent memory regions being isolated by one of said shallow trench isolation layers; memory transistors 11 formed in each of said memory regions to perform nonvolatile storage of data, each memory transistor including a floating gate 16 which is formed on said semiconductor substrate via a first gate insulating layer 56, a control gate 18 and 20

which is formed on said floating gate via a second gate insulating layer 58, and is strip-shaped, said control gate extending in another direction perpendicular to said one direction, and said control gate being common to said memory transistors, and two source/drain diffusion layers (12, 14) formed on the surface of said semiconductor substrate. Mehrad et al. does not disclose an oxide layer covering both sides of the gate stacks 50, sidewalls of a first silicon nitride layer covering both sides of said floating gate and said control gate of each of said memory transistors, and layers of second silicon nitride layer each covering upper surfaces of said control gate and surfaces of said sidewalls of each of said transistors so that the source/drain layers are exposed. Mori discloses a nonvolatile semiconductor memory device (Fig. 2) comprising multi-layered insulating layers covering the gate stacks and the substrate, wherein an oxide film 29 formed on the sides of the floating gate 23 and the control gate 25 and the substrate, oxide layer 37 formed on a substrate and on both sides of each floating gate 23 and both sides of each control gate 25; sidewalls 30 of first silicon nitride layer over said oxide layer; and a second silicon nitride layer 41 covering surfaces of the control gate, a source diffusion layer, a drain diffusion layer and sidewalls 30 so that the source/drain diffusion layers are exposed. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate the multi-layered insulating layers of Mori covering the gate stacks 50 of Mehrad et al. in order to inhibit loss of electrons from floating gate.

The claim limitations "at the time of the etching" and "being removed by etching" are taken to be product by process limitations which do not carry weight in claims drawn

to structure. In a product-by-process claim, it is the patentability of the claimed product and not of the recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. Also, a product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a " product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehrad et al. (USPN 6,071,779) in view of Mori (JP 407161848) as applied to claim 18 above, and further in view of Sato (USPN 5,962,890).

The combined references as described above does not disclose silicide layers formed on the control gate and source/drain diffusion layers. Sato discloses metal silicide films (102a, 109a, 110a) formed on the surfaces of a control gate and source/drain diffusion layers (109 and 110). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to form silicide layers

as taught by Sato on the control gate and source/drain diffusion layers (12, 14) of Mehrad et al. in order to reduce contact resistance.

Regarding claim 20, the modified Mehrad et al. discloses the drain diffusion layer 14 connected to a bit line 26 via the metal silicide film and the source diffusion layer 12 connected to a common source line 24 via the metal silicide film respectively.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mehrad et al. (US 6,071,779) in view of Mori (JP 407161848) as applied to claims 18 above, and further in view of Santin et al. (US 5,907,171).

The modified Mehrad et al. as described above does not explicitly disclose at least one of a low-voltage MOS transistor and a high-voltage MOS transistor formed as a peripheral circuit. It is conventional to form low-voltage transistor and high-voltage transistor as a peripheral circuit of a memory array to select and drive memory cells during circuit operations, as shown for example by Santin et al. Therefore, the incorporation of the conventional features into the modified Noda et al. would have been prima facie obvious.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F Tran whose telephone number is (703) 308-4108. The examiner can normally be reached on 8:00AM - 4:30PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

tt
November 25, 2002

Thien Tran
Patent Examiner
Technology Center 2800